ECE 413: Intro to VLSI

Assignment 1: Transistor Layout Introduction

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Honor Code:

I have neither given nor received unauthorized assistance on this graded report.

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NMOS

The following figure shows an NMOS transistor layout.

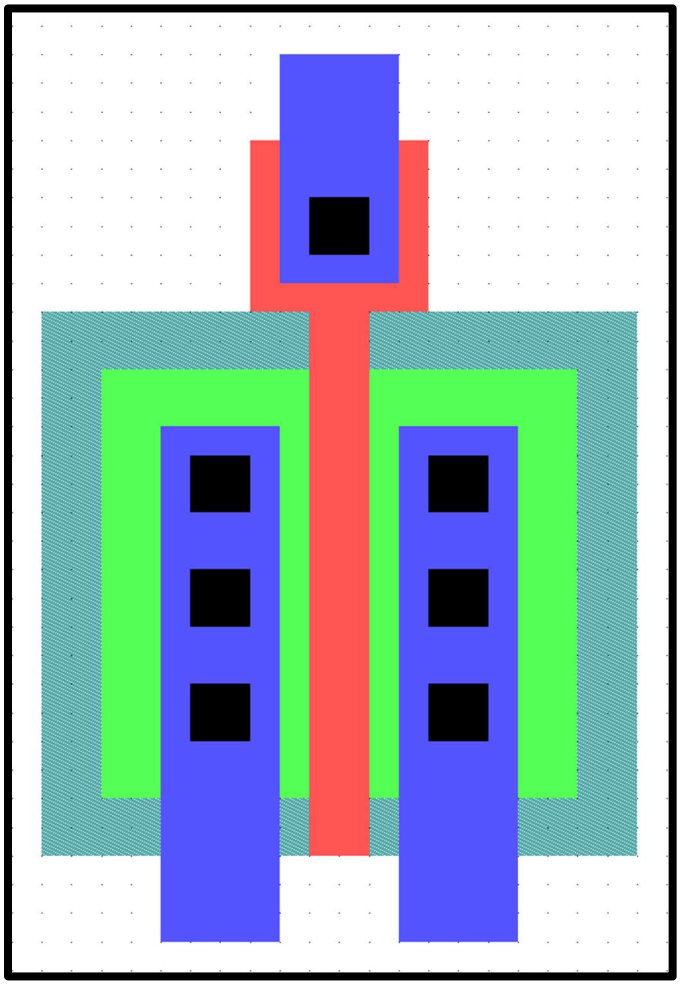

Figure-1: NMOS

Here are the resulting cross section views for the NMOS transistor shown above.

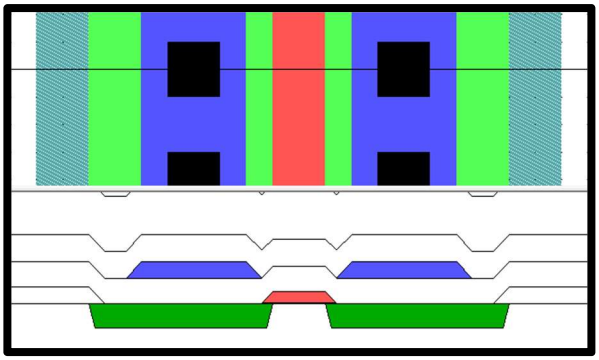

Figure-2: Horizontal Cross-Section of NMOS

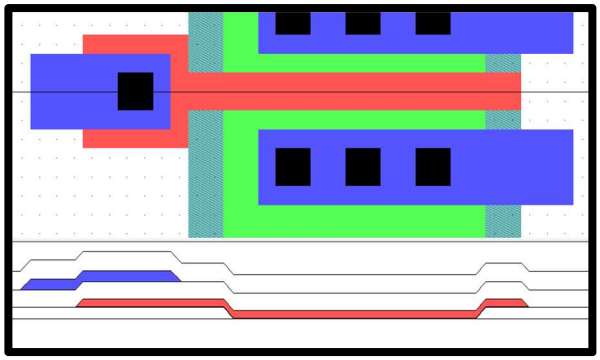

Figure-3: Vertical Cross-Section of NMOS

PMOS

The following figure shows a PMOS transistor layout (noting the N-Well layer on top of the substrate).

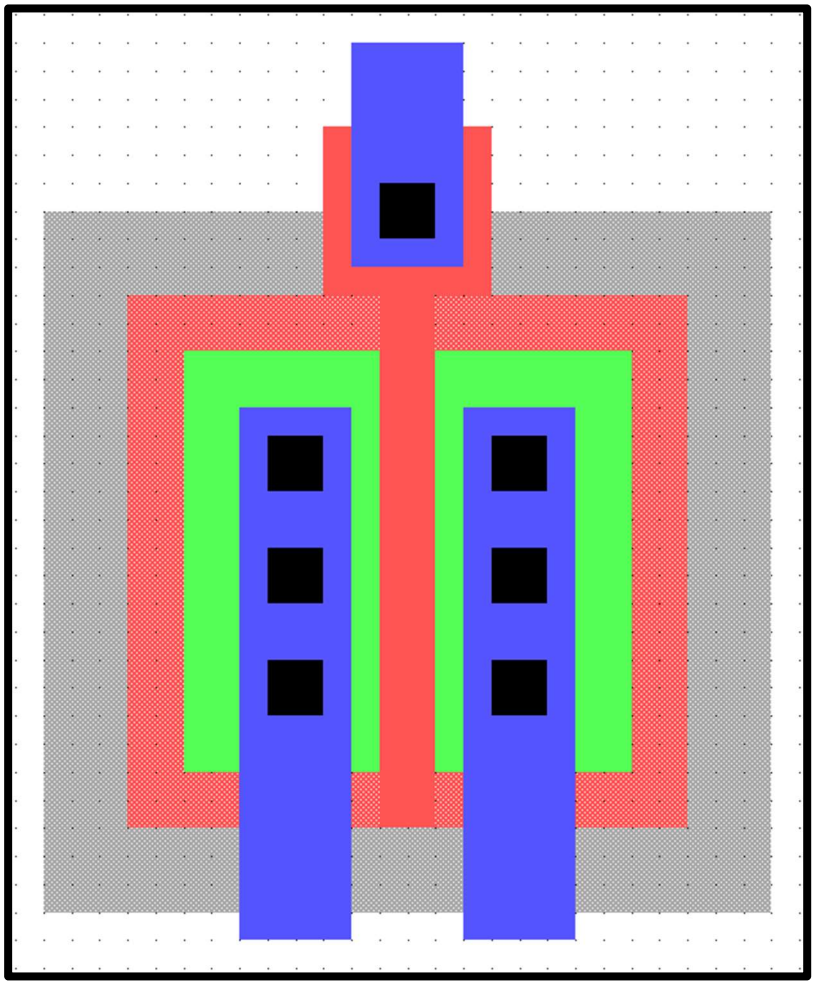

Figure-4: PMOS

Here are the resulting cross section views for the PMOS transistor shown above.

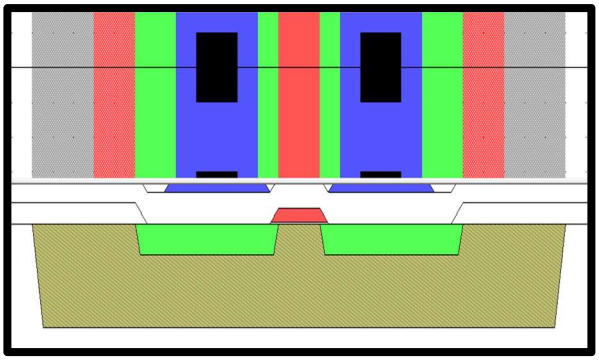

Figure-5: Horizontal Cross-Section of PMOS

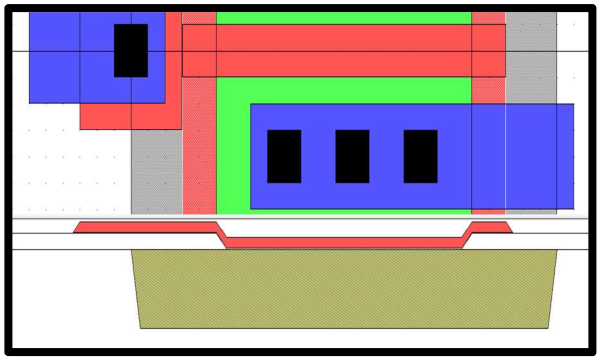

Figure-6: Vertical Cross-Section of PMOS

CMOS Inverter

The following figure shows a CMOS Inverter transistor layout made from the NMOS and PMOS. Note that the PMOS transistor is always connected to power, while the NMOS transistor is always grounded.

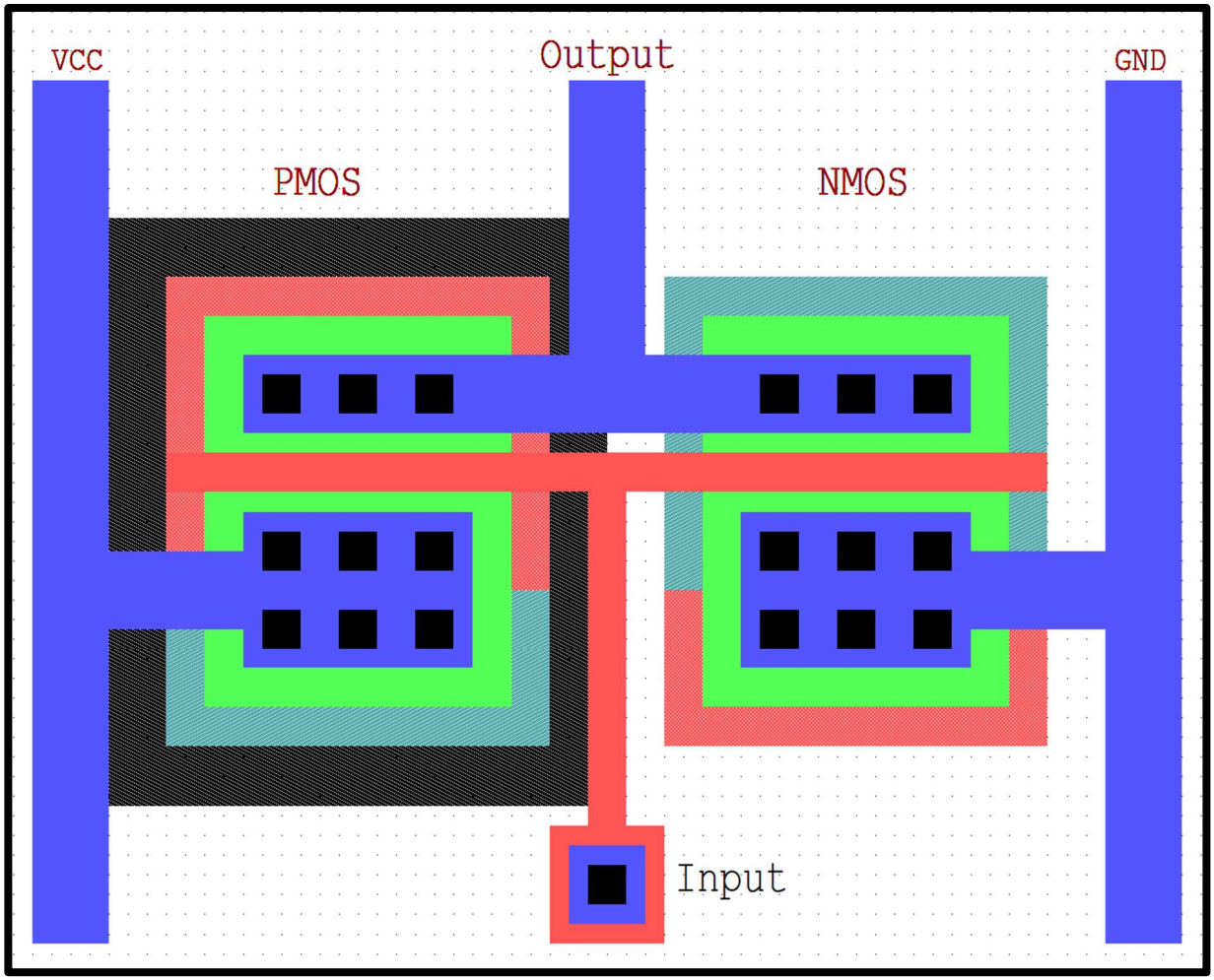

Figure-7: CMOS Inverter

Here are the resulting cross section views for the CMOS Inverter transistor shown on the previous page.

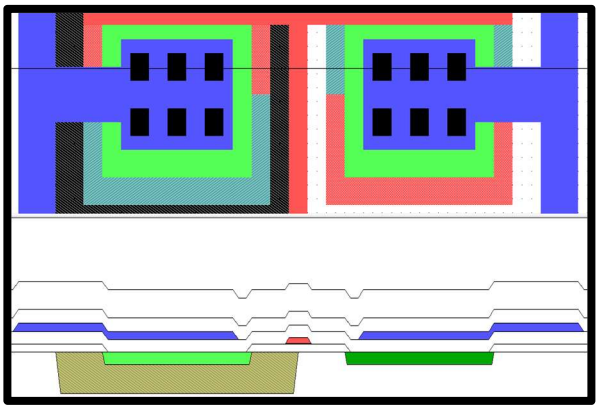

Figure-8: Horizontal Cross-Section of CMOS

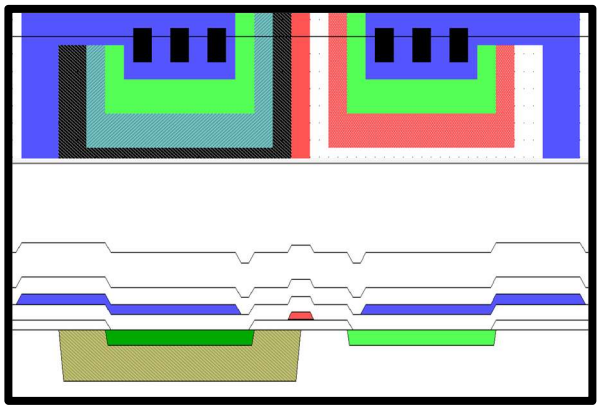

Figure-9: Horizontal Cross-Section of CMOS

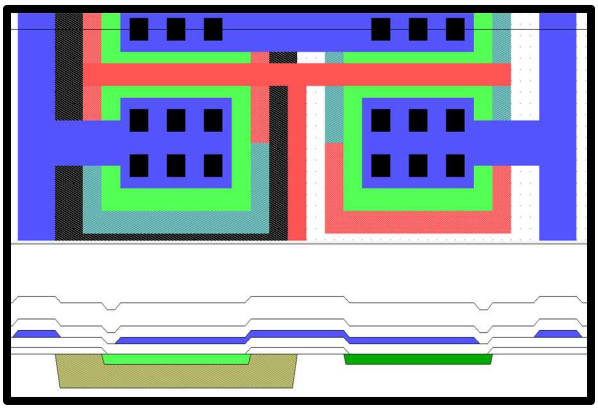

Figure-10: Metal1 Cross-Section of CMOS

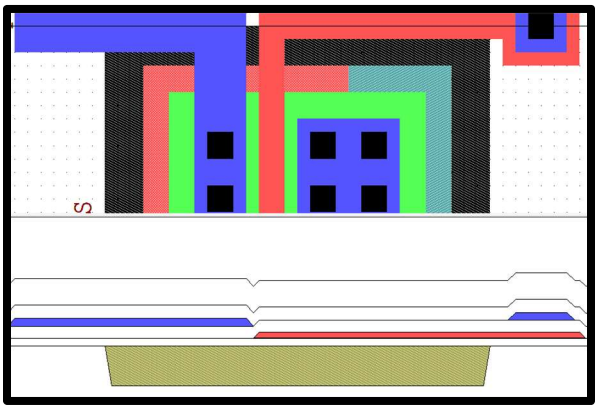

Figure-11: I/O Cross-Section of CMOS

Cascaded CMOS Inverters

The following figure shows three cascaded CMOS Inverter transistors. Note that the outputs of the prior CMOS drive the inputs of the following CMOS from left to right.

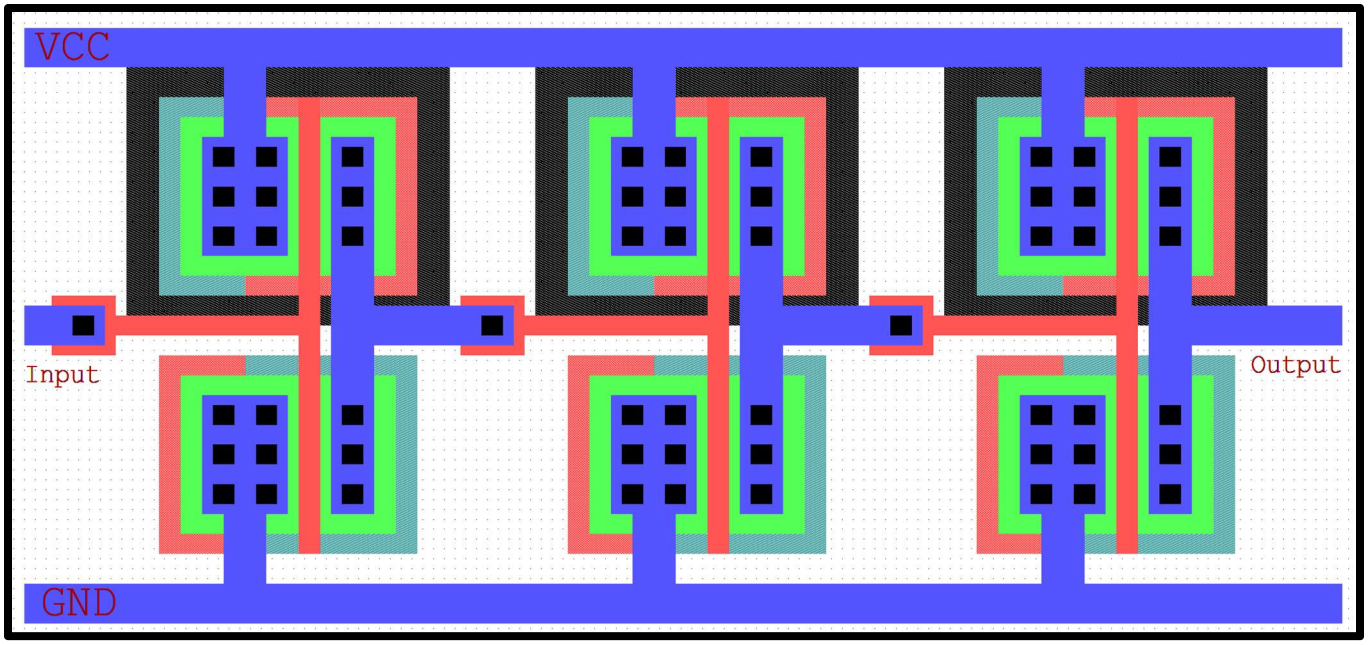

Figure-12: Cascaded CMOS Inverters

Here are the resulting cross section views for the cascaded CMOS Inverters as shown above.

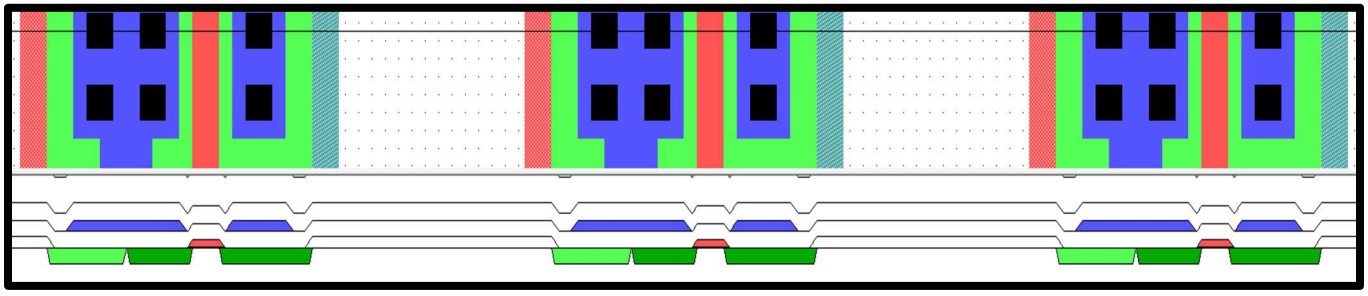

Figure-13: Horizontal Cross-Section of CMOS Inverter

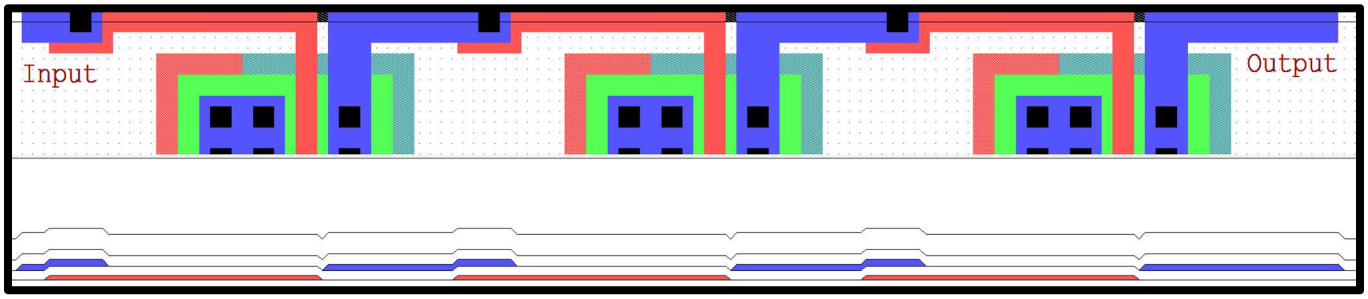

Figure-14: Horizontal Cross-Section of CMOS Inverter

DRC Files

The DRC files for the simulations are as follows:

###Procedures

Figure-15: NMOS DRC File (total errors = 0)

Figure-16: PMOS DRC File (total errors = 0)

Figure-17: CMOS Inverter DRC File (total errors = 0)

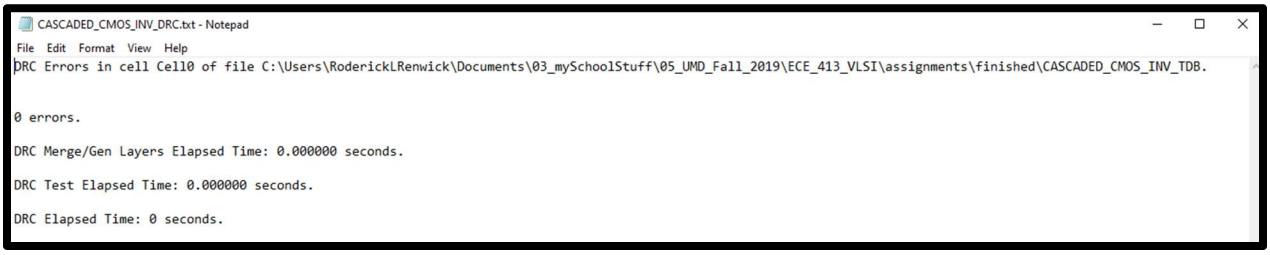

Figure-18: Cascaded CMOS Inverters DRC File (total errors = 0)

Conclusion

Overall I think that this simulation is a fantastic way to learn about transistors and makes the topic very fun to learn about. I am enjoying the hands-on approach to constructing and design these transistors and I believe that it helps solidify the concepts immensely.